AMENDMENTS

In the Claims:

1. (Currently Amended) A method of manufacturing a power transistor circuit, comprising carrying out the following steps in the enumerated order:

(1) ~~securing~~ providing ~~a die to~~ a substrate, said substrate comprising a pre-assembled power transistor circuit including ~~the~~ a die secured to said substrate comprising a transistor having an input terminal, ~~the substrate comprising~~ at least one input matching element and at least one input signal lead;

(2) measuring a performance characteristic of the transistor before connecting the transistor with the input matching element and input signal lead by means of a test network comprising connections with known inductances;

(3) using one or more wires to electrically couple the transistor input terminal to an input matching element, an input signal lead, or both; and

(4) setting the impedance of the one or more wires based at least in part on the measured transistor performance characteristic from step (2).

2. (Previously Presented) The method of claim 1, wherein the performance characteristic is defined, at least in part, by one or more of input capacitance, impedance, gain flatness, and signal phase shift.

3. (Previously Presented) The method of claim 1, wherein the impedance of the one or more wires is set by selecting a number of wires used to make at least one electrical connection of the transistor circuit.

4. (Previously Presented) The method of claim 1, wherein the impedance of the one or more wires is set by selecting a length of at least one wire used to make at least one electrical connection of the transistor circuit.

5. (Currently Amended) A method of manufacturing a power transistor circuit, comprising carrying out the following steps in the enumerated order:

(1) ~~securing a die to~~providing a substrate, said substrate comprising a pre-assembled power transistor circuit including ~~the~~ a die secured to said substrate comprising a transistor having an output terminal, ~~the substrate comprising~~ at least one input matching element and at least one input signal lead;~~;~~

(2) measuring a performance characteristic of the transistor before connecting the transistor with the input matching element and input signal lead by means of a test network comprising connections with known inductances;

(3) using one or more wires to electrically couple the transistor output terminal to an output matching element, an output signal lead, or both; and

(4) setting the impedance of the one or more wires based at least in part on the measured transistor performance characteristic from step (2).

6. (Previously Presented) The method of claim 5, wherein the performance characteristic is defined, at least in part, by one or more of output capacitance impedance, gain flatness, and signal phase shift.

7. (Previously Presented) The method of claim 5, wherein the impedance of the one or more wires is set by selecting a number of wires used to make at least one electrical connection of the transistor circuit.

8. (Previously Presented) The method of claim 5, wherein the impedance of the one or more wires is set by selecting a length of at least one wire used to make at least one electrical connection of the transistor circuit.